DPA-10-1-40 Digital Pulse Amplifier System

Introduction

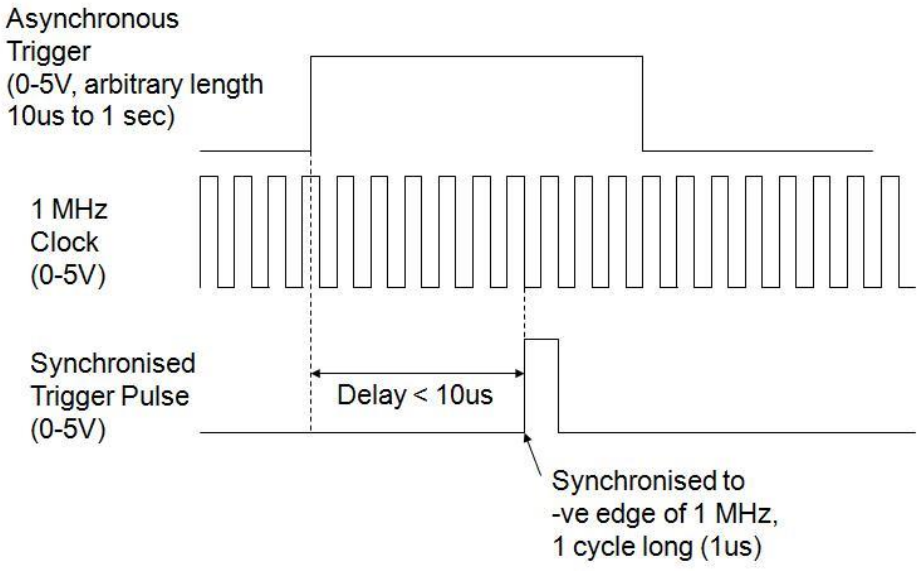
Precision Test Systems designs bespoke products, even in small quantities such as a one-off.

This application note describes one such design.

The customer gave us a design specification as follows:

- Design a pulse distribution system. The quantity was just one unit.
- Accept a 10 MHz sinewave signal at a level from +7 to +20 dBm.
- Generate multiple isolated 10 MHz outputs. The phase noise of these outputs to be -110 dBc @ 1 Hz offset with a -165 dBc/Hz noise floor.
- Also generate forty isolated 1 MHz squarewave outputs. Outputs to be differential and drive TTL voltages into twisted pairs.
- Synchronize the rising edge of a digital trigger input signal with the 1 MHz clock falling edge.
- Distribute forty synchronized trigger signals

Timing Diagram



The above timing diagram shows the relationship of the output signals.

- A 1 MHz clock is derived from the external 10 MHz input. It is then buffered and distributed to forty differential TTL outputs.
- When the asynchronous trigger pulse is received, a trigger pulse is generated with 10 µs, This trigger pulse has its rising edge synchronized to the 1 MHz's falling edge. The timing error to be < 10 ns.
- The trigger pulse width to be one cycle of the 1 MHz squarewave.
- The timing error of all 80 outputs to be < 10 ns.
- The trigger pulse is buffered and distributed to forty TTL differential outputs.
- An internal 10 MHz ultra low phase noise back-up oscillator was also to be provided. In the event of the external 10 MHz being removed, this internal 10 MHz would be immediately switched in.

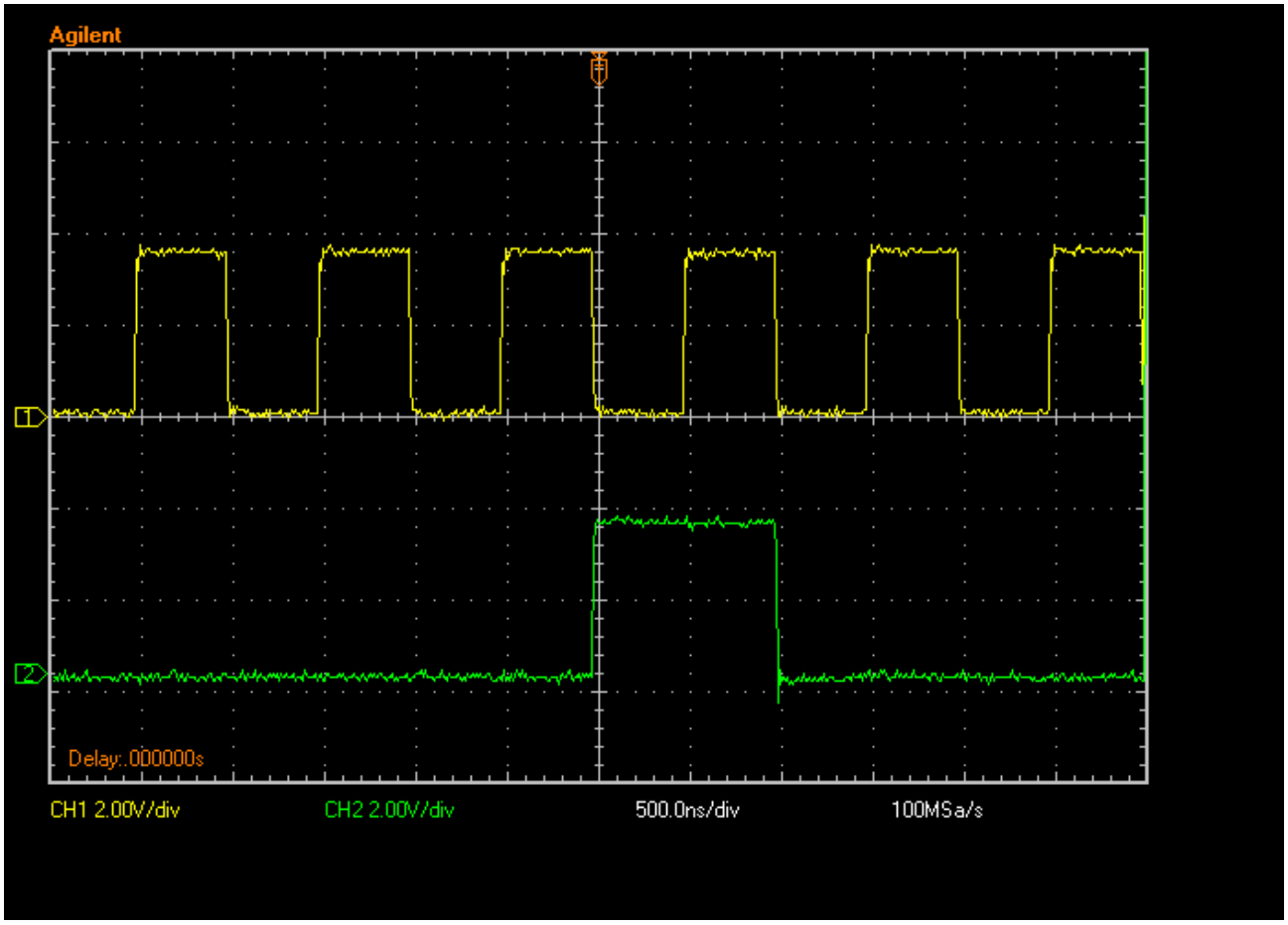
Picture of wiring inside the actual unit

Results

The final unit met all the customers' requirements and most specifications were exceeded.

Timing Results

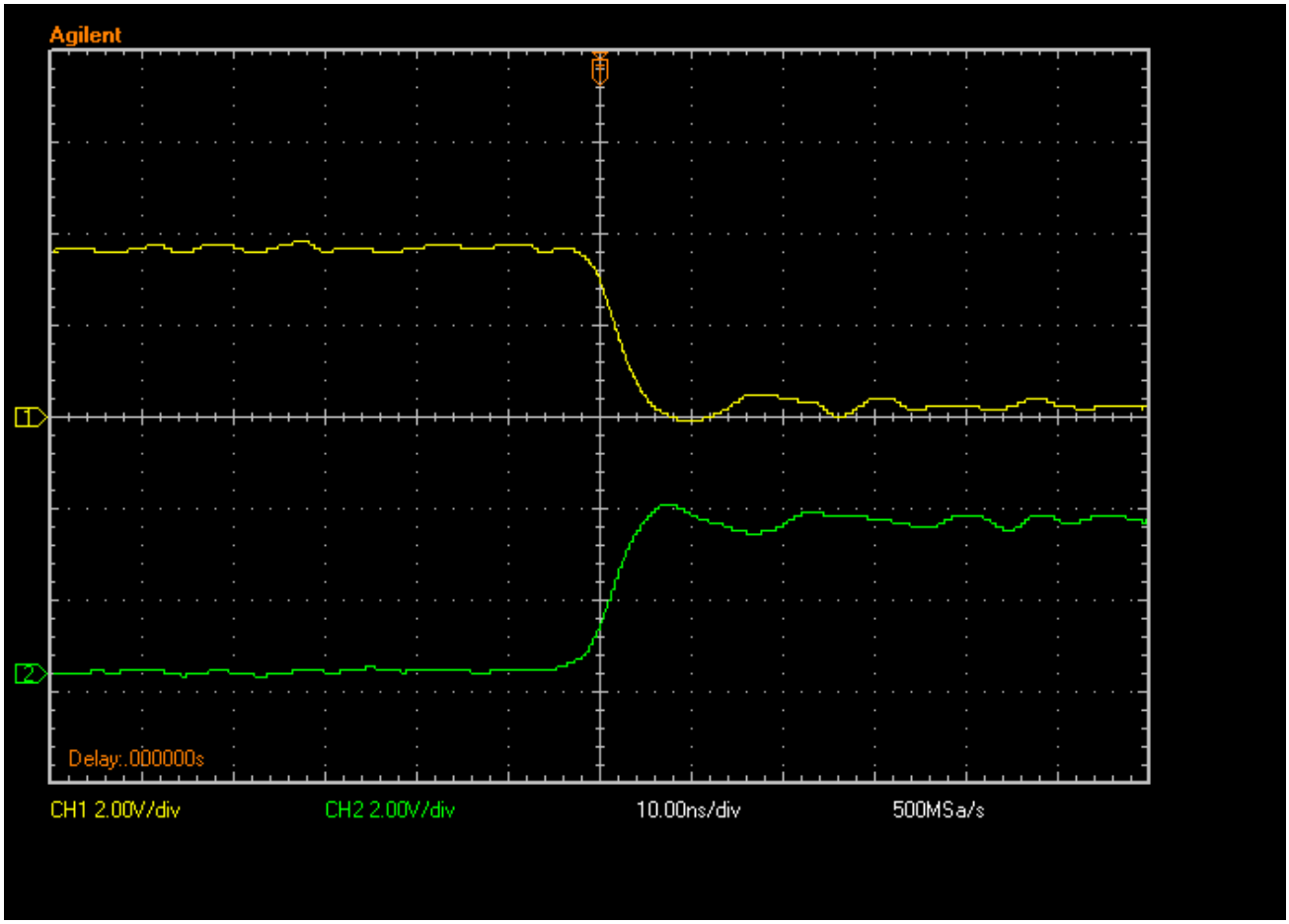
In the pictures below the yellow trace is the 1 MHz squarewave. The green trace is the trigger output pulse. As can be seen the trigger pulse's rising edge is aligned to the 1 MHz's falling edge. The error was < 6 ns on any of the 40 outputs and typically < 2 ns.



Zoomed timing waveform.

Here we see that the timing error was a few ns. Worse case error of any output was 5.7 ns.

Zoomed in version of the above picture



Phase Noise of the 10 MHz buffered outputs

The plot below shows the final phase noise of the internal 10 MHz buffered output. The result below includes the reference's phase noise. So actual phase noise is 3 dB lower than this. So we achieved -112 dBc/Hz at 1 Hz offset and a -166 dBc/Hz noise floor. The red spurious signals are related to the line frequency and are typical of any measurement made on units powered by AC 50 or 60 Hz.

Conclusion

All the customers' requirements were met and most were exceeded. The product was delivered and is now in use.

The customer purchased a second system a year later.